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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,199	10/16/2001	Byung-Gi Jung	1594.1010	3194

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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,199	JUNG, BYUNG-GI	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication app ars on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *Ocy. 16, 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: [all from Fig. 1] item numbers 105, 107a, 108, 113-120, 120a, and 122-128. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Figures 3-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by admitted prior art of Figures 1-2.

Regarding claim 1, the admitted prior art of figures 1-2 disclose a semiconductor device loading apparatus (100) for test handlers, comprising: a body (104) including a plurality of

pickup cylinders (112) provided with a plurality of vacuum adsorbers (111) for vacuum-sucking semiconductor (109) and transferring devices (109) to be tested, a space adjusting plate (121) for adjusting pitches of the vacuum adsorbers (111), and an elevation guiding means (107) for guiding lifting and lowering of the space adjusting plate (121); and a guide block fixing plate (108) formed to be separate from the body (104) for guiding the semiconductor devices (109) to be accurately positioned in pockets (110 shown in Fig. 3) of a test tray (110), respectively.

Regarding claim 2, the admitted prior art of figures 1-2 disclose said space adjusting plate (121) is provided with a plurality of guide slots (118) formed to allow spaces there between to be downwardly narrowed so as to adjust pitches of the vacuum adsorbers (111), and said vacuum adsorbers (111) are each provided with a guide projection (not number but shown in Fig. 2) adapted to be inserted to one of the guide slots (118).

Regarding claim 3, the admitted prior art of figures 1-2 disclose said guide block fixing plate (108) is positioned to be downwardly spaced apart from the vacuum adsorbers (111) and upwardly spaced apart from the test tray (110), and is provided with guide blocks of a number equal to the number of the pockets (110a) of the test tray (110).

Regarding claim 4, the admitted prior art of figures 1-2 disclose said guide blocks (108) are each provided with an opening sized to be equal to a size of each of the semiconductor devices (109), and with a pair of guide pins downwardly extended from front and rear edges thereof.

Regarding claim 5, the admitted prior art of figures 1-2 disclose said guide pins (not numbered but shown in Figs) each have a diameter smaller than a diameter of each of the pin holes (110d) formed in front and rear edges of the pocket (110a), and are spaced apart from each

other by a space equal to a space between the pair of pin holes (110d).

Regarding claim 6, the admitted prior art of figures 1-2 disclose said openings each comprise an entrance portion formed on an upper surface of the guide block (108) and sized to be slightly larger than a size of each of the semiconductor devices (109) to easily receive the semiconductor device (109), an exit portion formed on a lower surface of the guide block (108) and sized to be substantially equal to a size of the semiconductor device (109) to allow the semiconductor device (109) to pass there through, and a guide portion formed between the entrance and exit portions and tapered from the entrance portion to the exit portion.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Baba (5290134), Nakamura et al (5772387), Kanno (5961168), Yamada et al (6163145), Bannai (6184675 and 6259247), Kress (6439631) and Fukasawa et al (6593761) disclose a method and apparatus for a test handler for semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
February 5, 2004

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800